In The Figures

Please Amend FIG. 3B in accordance with the enclosed proposed change to that Figure. Namely add the label –PRIOR ART—to the FIG. 3B.

In The Claims

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region, having an island shape, formed on the principal surface of said semiconductor substrate, wherein the second conductivity type region has an impurity concentration profile in a depth direction of the semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type region wherein said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and wherein said impurity concentration profile of said second conductivity type region, resulting from impurities of a second conductivity type has a gentle peak at a depth that is greater than a junction depth of said first conductivity type region;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type region to at least said second conductivity type region on said semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon filling said trench, such that said insulation film is located between said electrode portion and said inner wall surface.

3. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region formed on the principal surface of said semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type region;

a plurality of first trenches, each extending from a surface of said highly doped first conductivity type region to reach at least said second conductivity type region on said semiconductor substrate, thereby defining a channel portion on an inner wall surface of each of the first trenches;

an insulation film formed on the inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon filling each of the first trenches such that said insulation film is located between said electrode portion and said inner wall surface;

a plurality of second trenches formed to extend into but not through said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches;

a second conductivity type protrusion region, which protrudes downwardly, wherein the second conductivity type protrusion region forms a junction that is deeper than a junction of said second conductivity type region, the protrusion region being positioned beneath the second trench; and

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

34. (Once Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, wherein the trench MOS structure includes:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench;

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second trench extending into but not through the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and the protrusion region encompasses the second conductivity type doped region; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench.

38. (Once Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, comprising:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench; and

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer and being in an electrically floating state; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through a second trench, wherein the upper electrode is isolated from the second conductivity type island.

40. (Once Amended) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises the second trench located in the second conductivity type region and positioned away from the first trench, the protrusion region being positioned beneath the second trench.